

October 1987 Revised May 2002

MM74C00 • MM74C02 • MM74C04 Quad 2-Input NAND Gate • Quad 2-Input NOR Gate • Hex Inverter

General Description

The MM74C00, MM74C02, and MM74C04 logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 74 devices minimizes design time for those designers already familiar with the standard 74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to $\rm V_{CC}$ and GND.

Features

■ Wide supply voltage range: 3V to 15V

■ Guaranteed noise margin: 1V

 \blacksquare High noise immunity: 0.45 $\rm V_{CC}$ (typ.)

■ Low power consumption: 10 nW/package (typ.)

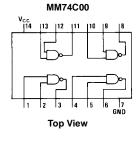
■ Low power: TTL compatibility: Fan out of 2 driving 74L

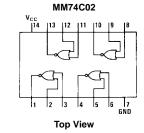
Ordering Code:

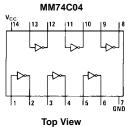
Order Number	Package Number	Package Description				
MM74C00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow				
MM74C00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide				
MM74C02N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide				
MM74C04M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow				
MM74C04N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide				

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code

Connection Diagrams







Absolute Maximum Ratings(Note 1)

Power Dissipation (P_D)

Dual-In-Line 700 mW Small Outline 500 mW

Lead Temperature

(Soldering, 10 seconds) 300°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across the guaranteed temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units
CMOS TO CN	ios					•
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 5.0V	3.5			V
		V _{CC} = 10V	8.0			
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 5.0V			1.5	V
		V _{CC} = 10V			2.0	
V _{OUT(1)}	Logical "1" Output Voltage	$V_{CC} = 5.0V, I_{O} = -10 \mu A$	4.5			V
		$V_{CC} = 10V$, $I_{O} = -10 \mu A$	9.0			
V _{OUT(0)}	Logical "0" Output Voltage	$V_{CC} = 5.0V, I_{O} = 10 \mu A$			0.5	V
		$V_{CC} = 10V, I_{O} = 10 \mu A$			1.0	
I _{IN(1)}	Logical "1" Input Current	V _{CC} = 15V, V _{IN} = 15V		0.005	1.0	μΑ
I _{IN(0)}	Logical "0" Input Current	V _{CC} = 15V, V _{IN} = 0V	-1.0	-0.005		μΑ
Icc	Supply Current	V _{CC} = 15V		0.01	15	μΑ
LOW POWER	TO CMOS	•				
V _{IN(1)}	Logical "1" Input Voltage	74C, V _{CC} = 4.75V	V _{CC} – 1.5			V
V _{IN(0)}	Logical "0" Input Voltage	74C, V _{CC} = 4.75V			0.8	V
V _{OUT(1)}	Logical "1" Output Voltage	74C, $V_{CC} = 4.75V$, $I_{O} = -10 \mu A$	4.4			V
V _{OUT(0)}	Logical "0" Output Voltage	74C, $V_{CC} = 4.75V$, $I_{O} = 10 \mu A$			0.4	V
CMOS TO LO	W POWER	•				
V _{IN(1)}	Logical "1" Input Voltage	74C, V _{CC} = 4.75V	4.0			V
V _{IN(0)}	Logical "0" Input Voltage	74C, V _{CC} = 4.75V			1.0	V
V _{OUT(1)}	Logical "1" Output Voltage	74C, $V_{CC} = 4.75V$, $I_{O} = -360 \mu A$	2.4			V
V _{OUT(0)}	Logical "0" Output Voltage	74C, $V_{CC} = 4.75V$, $I_{O} = 360 \mu A$			0.4	V
	VE (see Family Characteristics Da	a Sheet) TA = 25°C (short circuit current)				
I _{SOURCE}	Output Source Current	$V_{CC} = 5.0V, V_{IN(0)} = 0V, V_{OUT} = 0V$	-1.75			mA
I _{SOURCE}	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V, V_{OUT} = 0V$	-8.0			mA
I _{SINK}	Output Sink Current	$V_{CC} = 5.0V, V_{IN(1)} = 5.0V, V_{OUT} = V_{CC}$	1.75			mA
I _{SINK}	Output Sink Current	V _{CC} = 10V, V _{IN(1)} = 10V, V _{OUT} = V _{CC}	8.0			mA

AC Electrical Characteristics (Note 2)

 $T_A = 25^{\circ}C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Тур	Max	Units
MM74C00, MM	//74C02, MM74C04	•	•	U		
t _{pd0} , t _{pd1}	Propagation Delay Time to	V _{CC} = 5.0V		50	90	
	Logical "1" or "0"	V _{CC} = 10V		30	60	ns
C _{IN}	Input Capacitance	(Note 3)		6.0		pF
C _{PD}	Power Dissipation Capacitance	Per Gate or Inverter (Note 4)		12		pF

Note 2: AC Parameters are guaranteed by DC correlated testing.

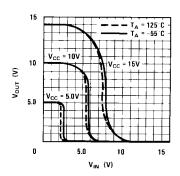
Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device.

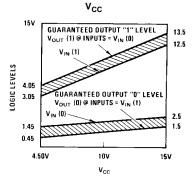
For complete explanation see Family Characteristics Application Note—AN-90.

Typical Performance Characteristics

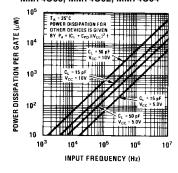
Gate Transfer Characteristics



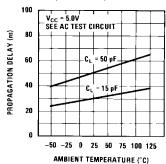
Guaranteed Noise Margin Over Temperature vs.



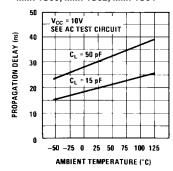
Power Dissipation vs. Frequency MM74C00, MM74C02, MM74C04



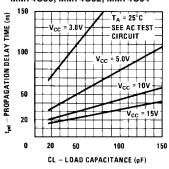
Propagation Delay vs. Ambient Temperature MM74C00, MM74C02, MM74C04



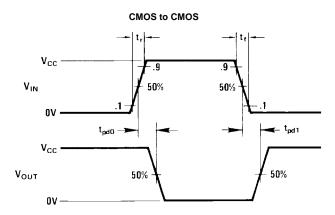
Propagation Delay vs. Ambient Temperature MM74C00, MM74C02, MM74C04

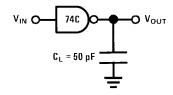


Propagation Delay Time vs. Load Capacitance MM74C00, MM74C02, MM74C04

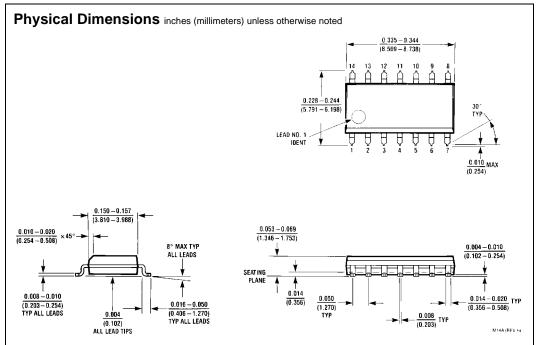


Switching Time Waveforms and AC Test Circuit





Delays measured with input $t_{\rm r},\,t_{\rm f} \leq 20$ ns.



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\frac{0.630 - 8.128}{(7.620 - 8.128)}$ $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 0.060 4° TYP Optional (1.651) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ (1.905 ± 0.381) (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) (0.356 - 0.584)0.050 ± 0.010 TYP 0.325 ^{+0.040} -0.015 (1.270 - 0.254)8.255 + 1.016

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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N144 (REV.F)